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Optimized Development Environment (ODE) for e20xx/e2xx
Intelligent onboard processing

Training Professionals and Researchers on Future Intelligent On-board Embedded Heterogeneous Processing

Description

The Optimized Development Environment (ODE) is a mini-ITX compatible rapid engineering platform for the e2000 and e2100 reliable hetereogeneous compute products. The ODE provides flexible software development based on the Deep Delphi™ software library. Deep Delphi™ include Lightweight Ubuntu 16.04 LTS (AMD64) with UNiLINK kernel driver for extended IO and health monitoring through FPGA. Open source Linux libraries provide support for amdgpu kernel driver, AMD IOMMU kernel driver, AMD DDR RAM memory Error Correction Code (ECC), OpenGL, Vulkan, OpenCL (patched Mesa/Clover), Robotic Operating System (ROS), Open Computer Vision (OpenCV), and optional machine learning libraries (e.g. Caffe, Theano, TensorFlow, PlaidML).

Tailoring beyond the standard FPGA functionality, requires additional FPGA design services by Troxel Aerospace Industries, Inc.

FreeRTOS support is optional and may change the demo software flow between AMD SOC and FPGA. Software developed on ODE is compatible with the Deep Delphi iX5 platform.

SPECIFICATION HIGHLIGHTS

Processing products	e20xx family e21xx family
Power input	ATX 4 pin (12 V) 802.3at Type 2, 30W, PoE (FPGA LAN port) ATX 20 pin (12, 5, 3.3 V) (Internal only)
Graphics	HDMI & LCD/LVDS
Storage	2×SATA v3.0 (6 Gbps) (1 x 120 GB SSD incl.) 1×MicroSD-Card/MMC
Board size	170 × 170 mm2 (mini-ITX compatible)
BIOS recovery	UNIBAP™ Safe Boot + SPI headers for DediProg.
Temp. range	0 °C to 40 °C
Development area (requires FPGA IP core tailoring by TAI)	24/48 Single/Differential GPIO, I2C, SPI, SERDES, 3.3 V, 5 V, 12 V, HW reset
Ethernet	2×1000Tbase LAN (AMD) 1×1000Tbase LAN (FPGA)
USB	2×USB3.0 (AMD SOC) 4×USB2.0 (AMD SOC)
PCIexpress®	1×4 lanes (v2) (Internal)
Serial Ports	2×RS232 (FPGA) 2×UART TTL (AMD)
Debug	AMD SmartProbe (Internal only) FPGA JTAG interface (Internal) FPGA ARM Cortex-M3 interface (internal)
CAN bus	CAN 2.0b (through FPGA)
Other	SPI, I2C, Health monitoring, fan control, HD Audio

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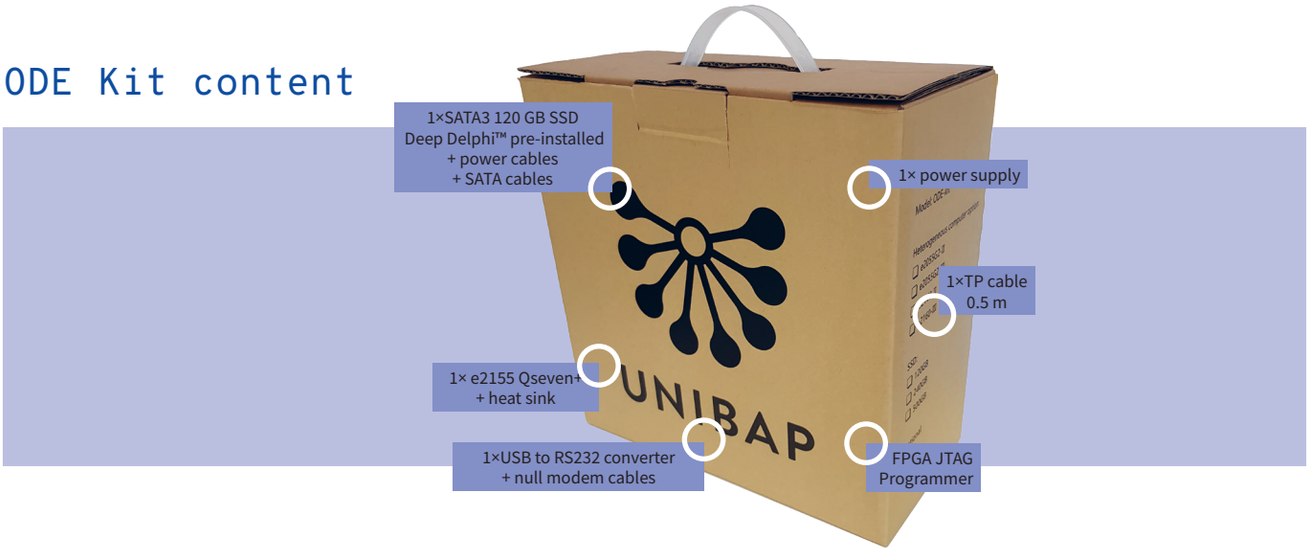
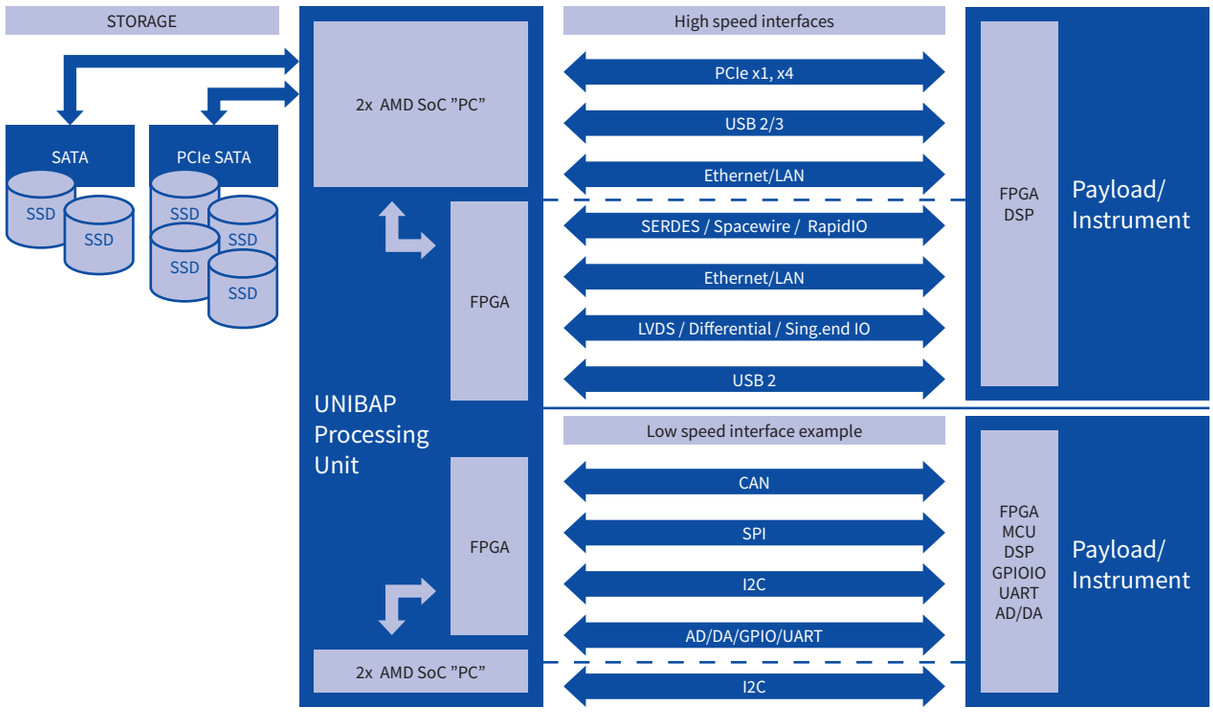
ODE Kit content



ODE system example

The ODE kit provides a wide range of high and low speed interface options that the user can use to prototype various configurations of interest. A summary of different options is shown in the illustration below. This example assumes an external PCIe SATA disk controller for expanded storage.



ODE system example overview

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